Dynamic Engineers Inc.
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**XO-5-7-2.5V-LVDS-xMHz**
LVDS10 to 1450MHz Clock Oscillator

## Features and Benefits

Frequency Range 10 MHz to 1450 MHz
Output Frequency to six decimal places
Output Frequency Examples: 12.688375 MHz ; 125.345678 MHz
7 mm x 5.0 mm x 1.80 mm ceramic SMD 6-pad
±50 ppm total stability over -40°C to 85°C
1 to 1.5 pico-second phase jitter ( 12KHz to 20 MHz )
LVDS outputs
2.5V supply

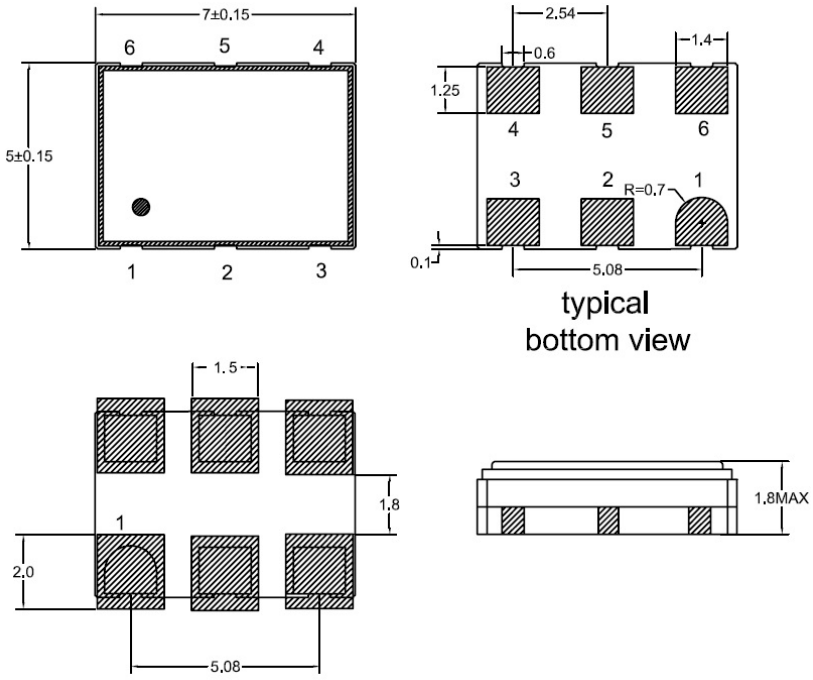
## Typical Applications

Gb Ethernet, SONET, Fibre channel, FPGA, and A/D clock reference devices

## Description

A new generation of low jitter / low power clock oscillators has been developed using the latest low noise integrated circuit topologies.

## Mechanical Drawing & Pin Connections




| Product | XO | VCXO |
|---|---|---|
| **Pad 1** | High Enable | Voltage Control |
| **Pad 2** | No Connection | High Enable |
| **Pad 3** | Ground | |
| **Pad 4** | CMOS: Output LVPECL, LVDS: Differential Output | |
| **Pad 5** | CMOS: No connection LVPECL, LVDS: Complementary Output | |
| **Pad 6** | Supply voltage | |

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## Specifications

| **General Specifications: at Ta=+25°C,** | | |
|---|---|---|
| **Output Logic Type** | LVDS | |
| **Frequency Range** | 10 ~ 1450 MHz | |
| **Load** | Differential | |
| **Power Supply Voltage ($V_{DD}$)** | $V_{DD}$ = +2.5V D.C. ± 5% | |
| **Output "High" Voltage; $V_{OH}$** | Voltage ($V_{OD}$) | 1.4 V Typical , 1.6 V max |
| **Output "Low" Voltage; $V_{OL}$** | Voltage ($V_{OD}$) | 1.1 V Typical , 0.9 V min. |
| **Frequency Stability** | ±50 ppm over -40°C to 85°C<br>Over all conditions | |
| **Duty Cycle** | 50% ± 5% | |
| **Rise Time (Tr)/Fall Time (Tf)**<br>(20% $V_{DD}$ – 80% $V_{DD}$) | 0.2nS. typ. 0.4nS. max. | |
| **Current Consumption**<br>$V_{DD}$ = +2.5V<br>All values are typical and over operating temperatures. | 100 MHz: 16 mA | |
| | 250 MHz: 18 mA | |
| | 500 MHz: 21 mA | |
| | 750 MHz:22 mA | |
| | 1 GHz:24 mA | |
| | 1.35 GHz: 26 mA | |
| **Current with Output Disabled** | 16 mA typical | |
| **Start-up Time** | 10 ms max. | |
| **Aging** | ±2 ppm max. first year at 25°C; ±10 ppm max. over 10 years | |
| **Output Enable Function** | | |
| **OE Pad Input**<br>**XOs: Pad 1**<br>**VCXOs: Pad 2** | 70% of $V_{DD}$minimum or no connection to enable output. LVCMOS/LVTTL level.<br>30% of $V_{DD}$maximum to disable output (high impedance). LVCMOS/LVTTL level. | |
| **Output Enable Time** | 200 ns max. | |
| **Output Disable Time** | 50 ns max. | |
| **Integrated Phase Jitter** | | |
| **Phase Jitter, rms**<br>**(12 KHz to 20 MHz)** | 1.0 pS typical; 1.5 pS max. | |
| **Phase Jitter, rms**<br>**(1.875 MHz to 20 MHz)** | < 100 fs | |
| **Environmental Performance Specifications** | | |
| **ROHS Status** | RoHS compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC) | |
| **Storage Temp. Range** | -55°C to 150°C | |
| **Humidity** | 85% RH, 85°C, 48 hours | |
| **Fine Leak / Gross Leak** | MIL-Std-883, method 1014, condition A / MIL-Std-883, method 1014, condition C | |
| **Solderability** | MIL-STD-202F method 208E | |
| **Reflow** | 260°C for 10 sec. 2X. | |
| **Vibration** | MIL-STD-202F method 204, 35G, 50 to 2000 Hz | |
| **Shock** | MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave | |
| **Resistance to Solvent** | MIL-STD-202, method 215 | |
| **Temperature Cycling** | MIL-STD-883, method 1010 | |
| **ESD Rating** | >2000 V (per MIL-STD-883, method 3015) | |

## Ordering Options:

**"x MHz " examples : 125.000000 MHz ; or 12.688375 MHz ; 1250.005600 MHz**

## Phase Noise Graphs

212 MHz LVDS output

1000 MHz LVDS output